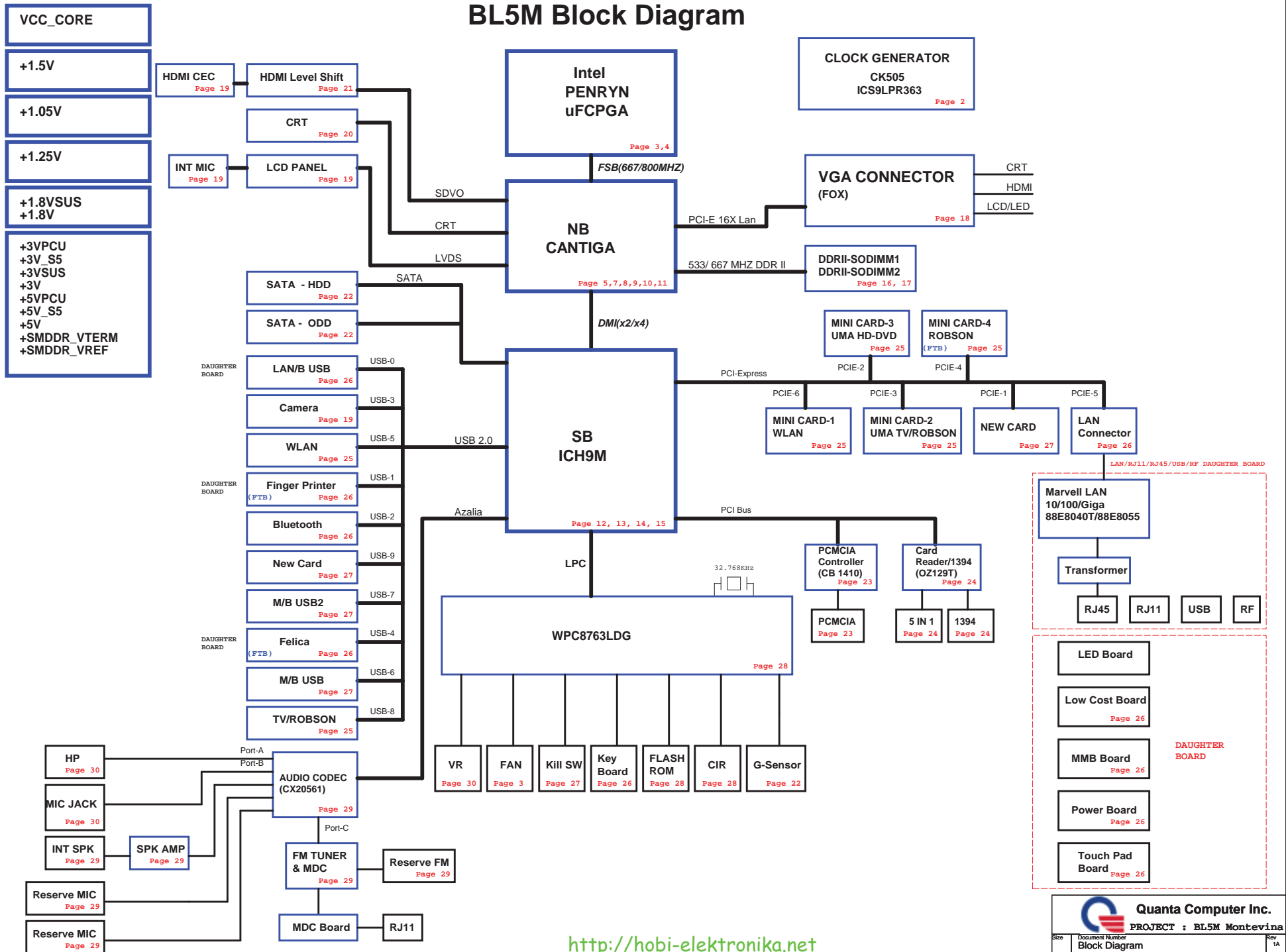
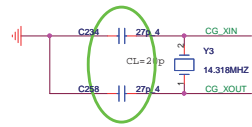


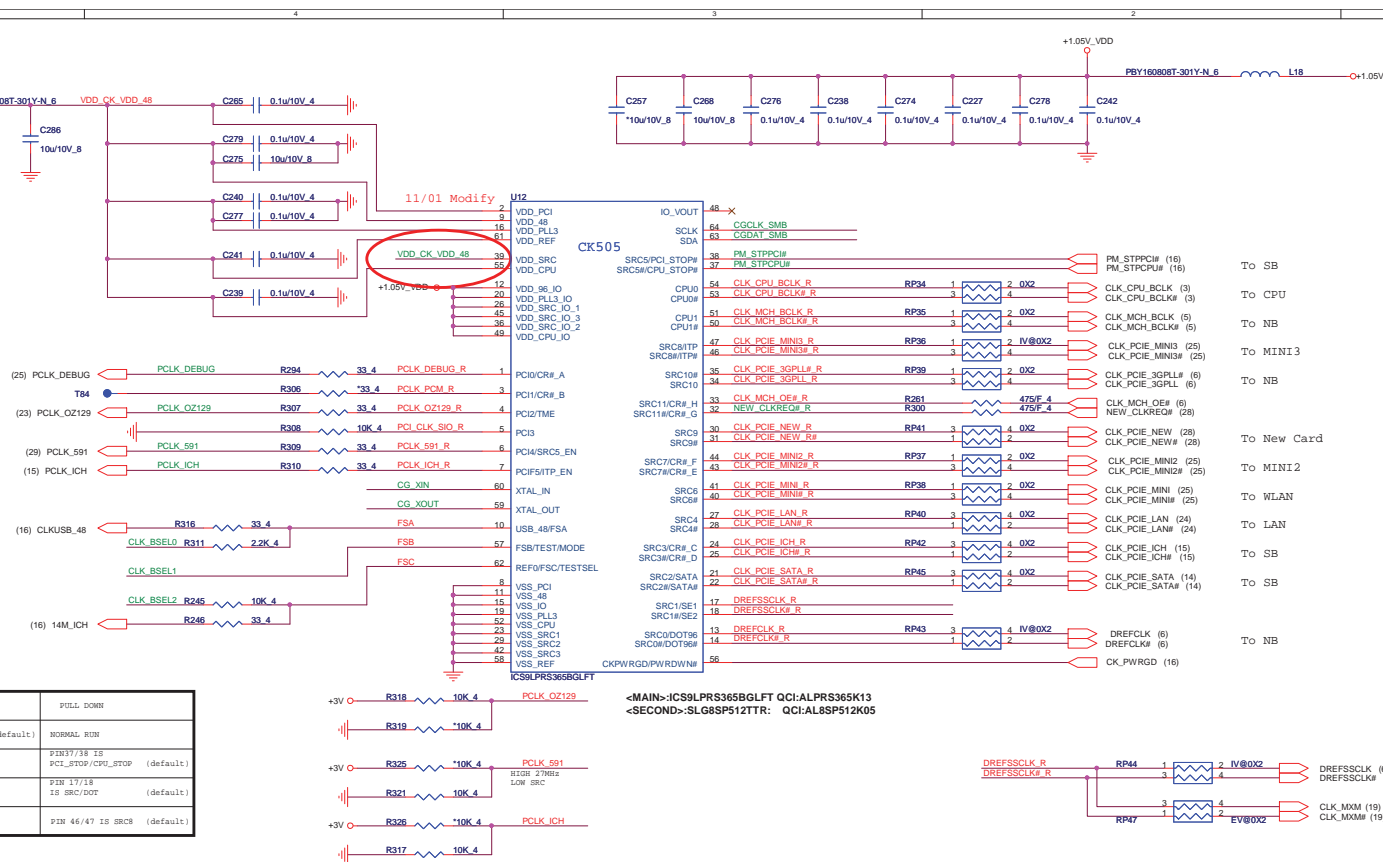
BL5M Block Diagram



Clock Generator



10/30 Change Value and need change PN



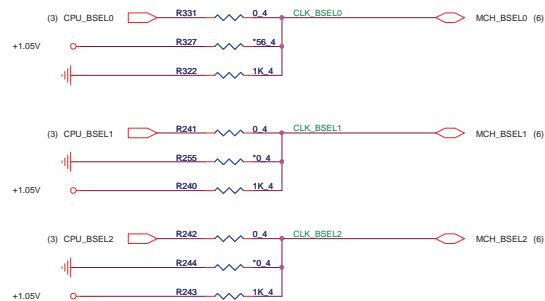
Reference	Description
IV@	INT VGA
EV@	EXT VGA

	P0212P0215 [ALPS9368E2]	PIN070T-606 [ALPO097806E]	FULL HIGH	FULL DOWN
Pin 4	P0C12,T2ME	P0C12,T2ME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	P0C1-3	P0C1-3,SBCSLR,SRCS internal PD	PIN37/38 IS SRCS	PIN37/38 IS P0C1_STOP/CPU_STOP (default)
Pin 6	P0C1-4,INTWR,SEL	P0C1-4,INTWR,SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SBCI_STOP (default)
Pin 7	P0CIP-5,ITP,SRCS	P0CIP-5,ITP,SRCS internal PD	PIN 46/47 IS CPUPTD	PIN 46/47 IS SRCS (default)

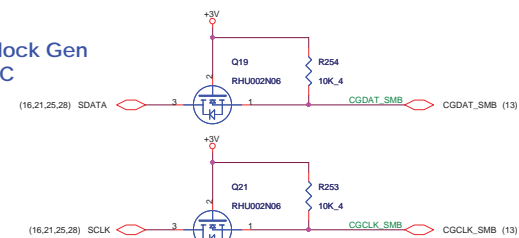
FREQ. SEL
TABLE

BSEL Frequency Select Table

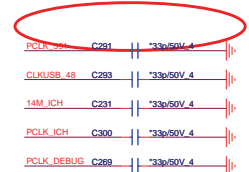
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz




Clock Gen I2C



11/01 Del C3195



 Quanta Computer Inc. PROJECT : BL5M Montevina		
Size	Document Number CLK. GEN./ CK505	Rev 1A
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BOM Option Table

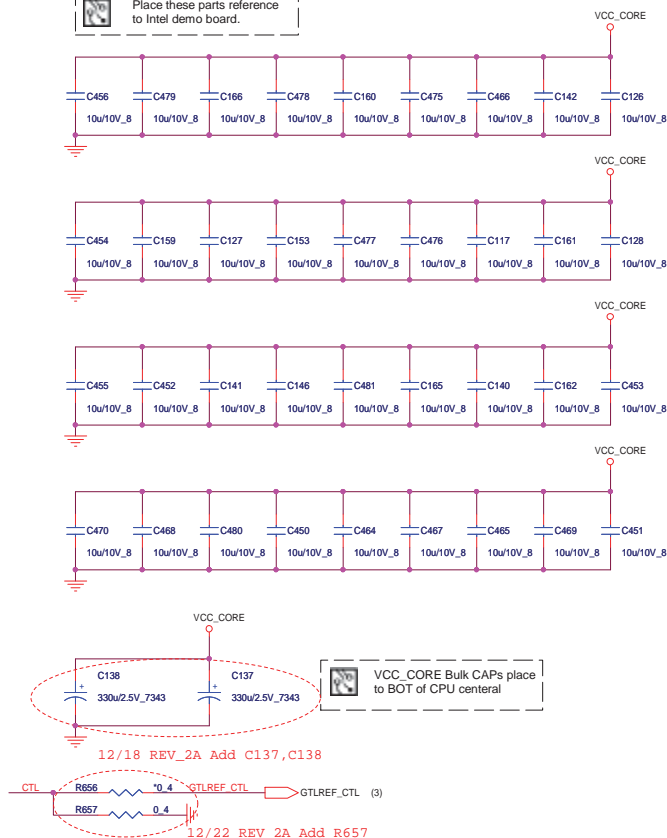
Reference	Description
N/A	N/A

Need NC 20PCS 10u before A1 BOM released(A0 all stuff)

Place these parts reference to Intel demo board.

Layout Note:
Inside CPU center cavity in 2 rows

U24D	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R5
A16	VSS[005]	VSS[086]	R2
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T28
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V2
C11	VSS[018]	VSS[099]	V25
C14	VSS[019]	VSS[100]	W1
C16	VSS[020]	VSS[101]	W4
C18	VSS[021]	VSS[102]	W23
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA5
D11	VSS[029]	VSS[110]	AA8
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA25
E6	VSS[036]	VSS[117]	AB1
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AC3
F11	VSS[046]	VSS[127]	AC6
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC11
F19	VSS[049]	VSS[130]	AC14
F2	VSS[050]	VSS[131]	AC16
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE4
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE2
M2	VSS[073]	VSS[154]	AF6
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF11
M25	VSS[076]	VSS[157]	AF13
N1	VSS[077]	VSS[158]	AF16
N4	VSS[078]	VSS[159]	AF18
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	AE25
		VSS[163]	AE25

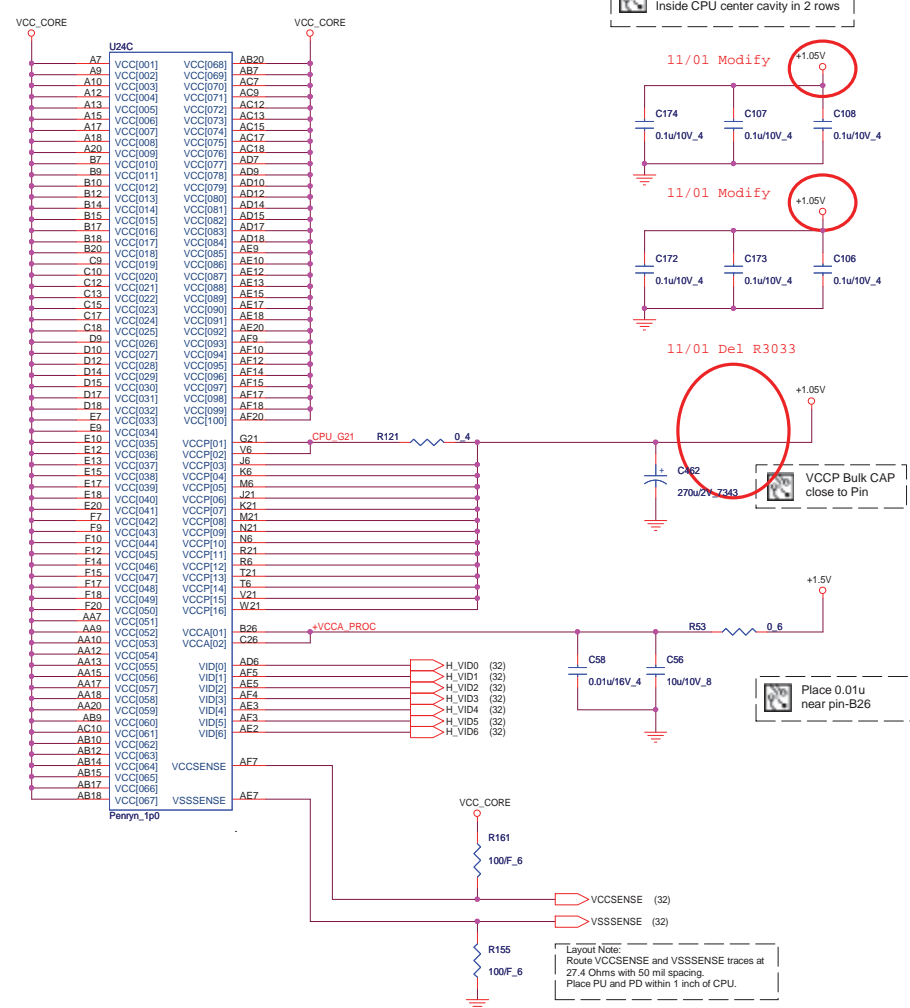


Penryn CPU Power Status and max current table

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	47A	Standard Voltage CPU
VCC_CORE	O	X	X	VID	50A	SV Design Target
VCC_CORE	O	X	X	VID	TBD	Extreme Edition CPU
VCC_CORE	O	X	X	VID	67A	EE Design Target
VCCA	O	X	X	+1.5V	130mA	
VCCP	O	X	X	+1.05V	4.5A	Before VCC Stable
VCCP	O	X	X	+1.05V	2.5A	After VCC Stable

(See Penryn EMTS Rev:1.0 Table 7,8 for voltage and current)

(See Penryn EMTS Rev:1.0 Table-3 for VID table)



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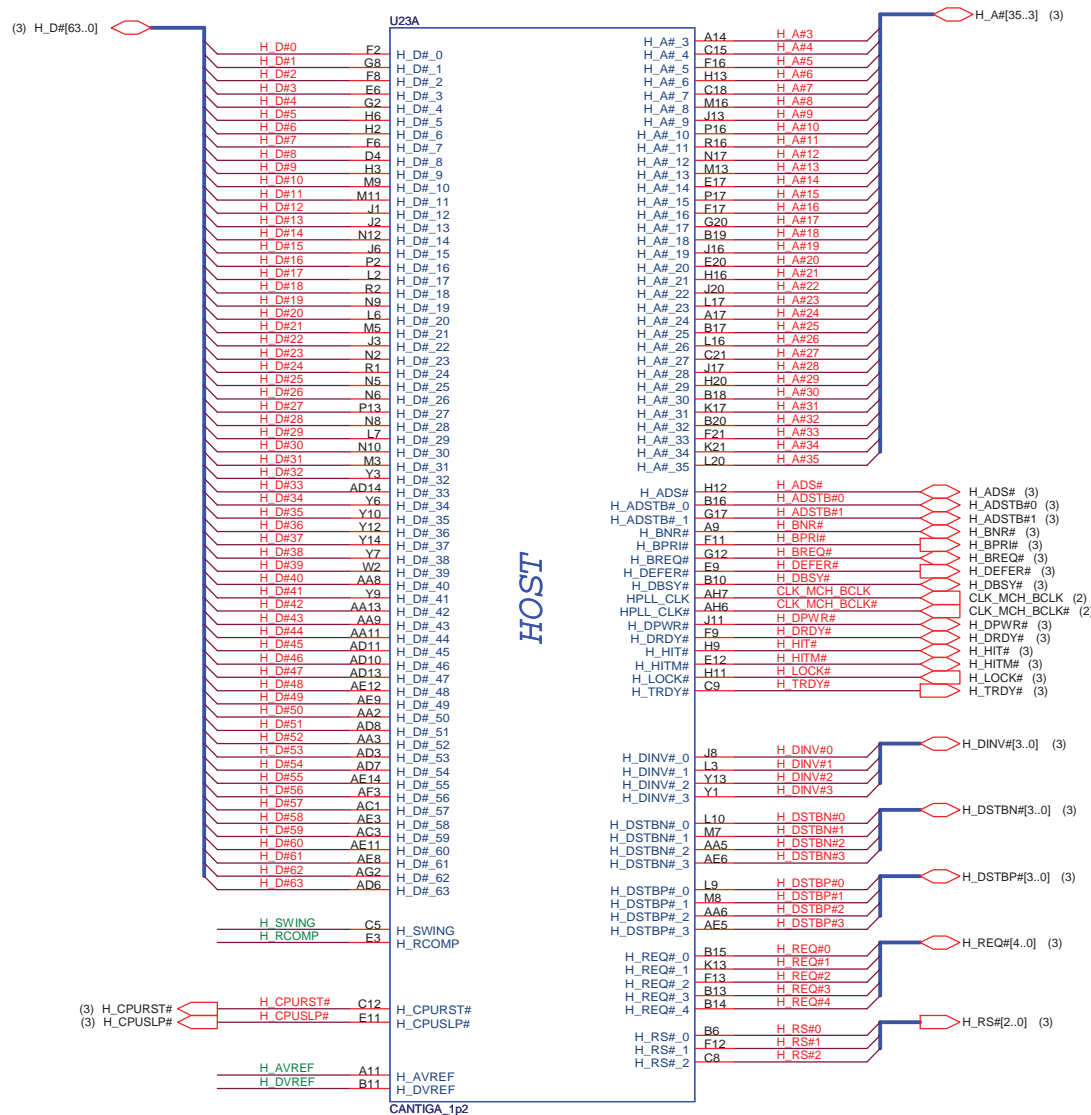
PROJECT : BL5M Montevina

Size	Document Number	Rev
	CLK_GEN / CK505	1A

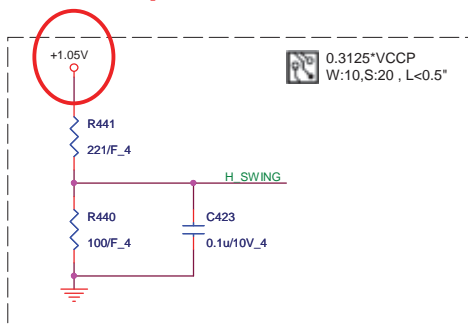
Date: Monday, March 10, 2008 Sheet 4 of 37

BOM Option Table

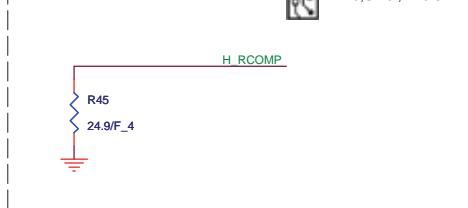
Reference	Description
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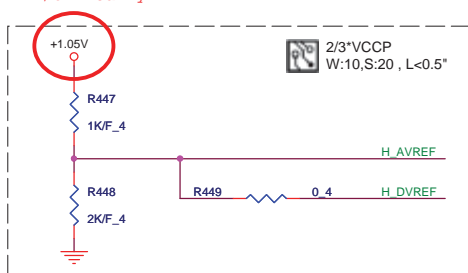
11/01 Modify



W:10,S:20, L<0.5"



11/01 Modify



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PROJECT : BL5M Montevina

Size	Document Number	Rev
	CLK. GEN/ CK505	1A

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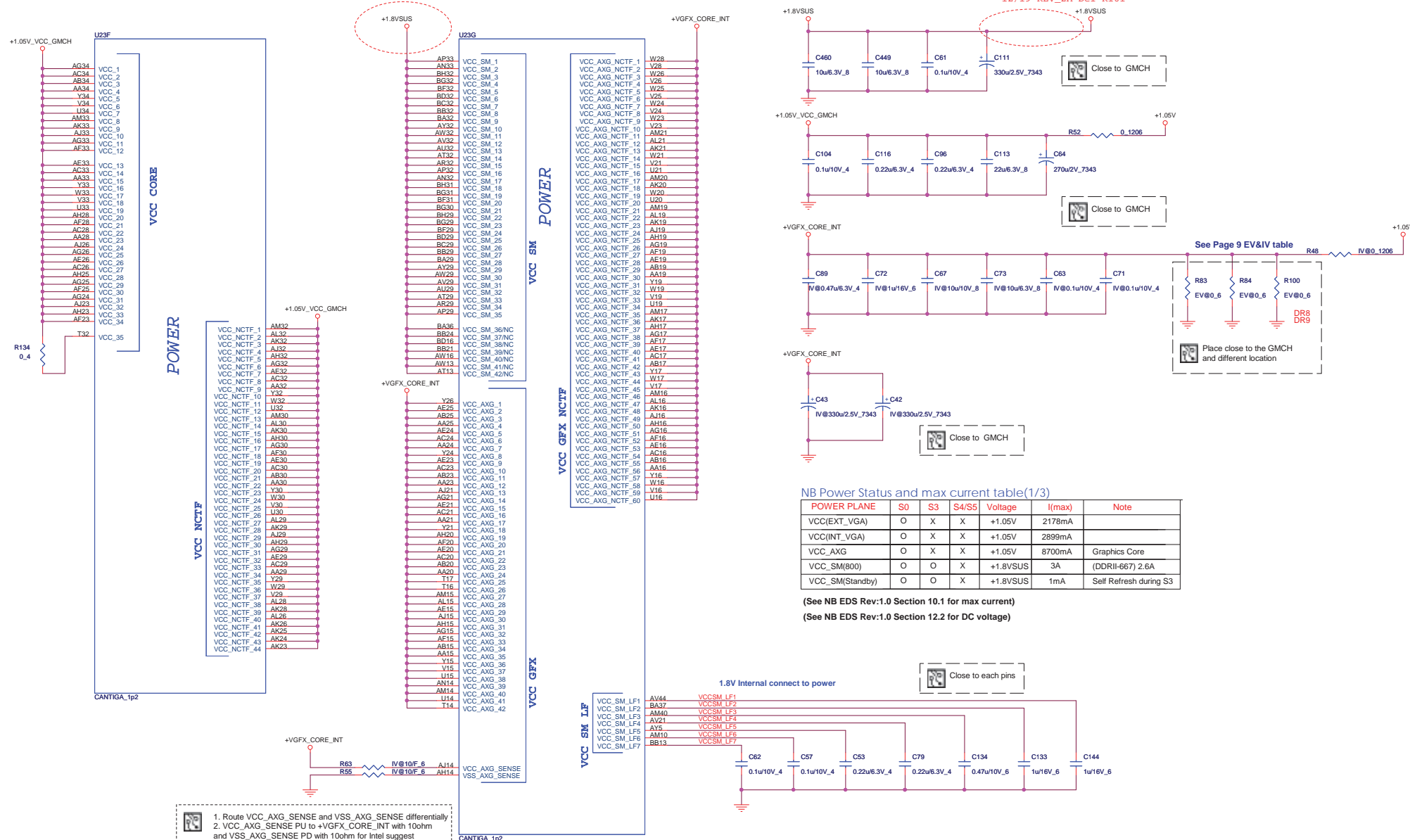


BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

12/19 REV_2A Chanhe net to +1.8VSUS

12/19 REV_2A Del R101



NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(B00)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

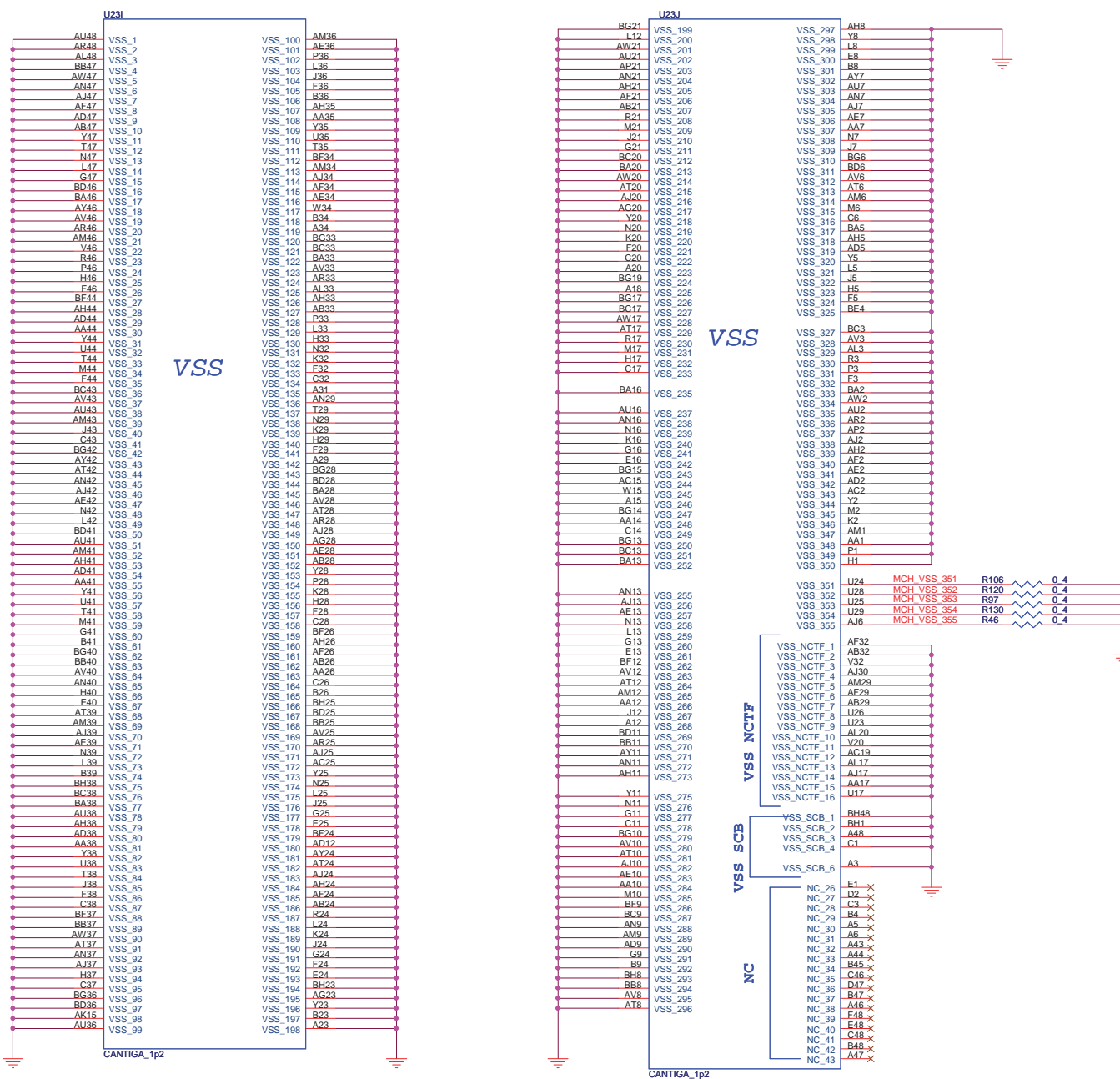
(See NB EDS Rev:1.0 Section 10.1 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

1.8V Internal connect to power

BOM Option Table

Reference	Description
N/A	N/A
















North Bridge Strap Pin Configuration Table

(See DG 1.0 P295 Table 184)
(See NB EDS 1.0 P187 Table 74)


BOM Option Table

Reference	Description
N/A	N/A

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	(6) MCH_CFG_5  R93 *4.02K/F_4	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	(6) MCH_CFG_6  R99 *10K/F_4	
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	(6) MCH_CFG_7  R98 *4.02K/F_4	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	(6) MCH_CFG_9  R454 *4.02K/F_4	
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)	(6) MCH_CFG_10  R455 *4.02K/F_4	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	(6) MCH_CFG_12  R76 *4.02K/F_4	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	(6) MCH_CFG_13  R77 *4.02K/F_4	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	(6) MCH_CFG_16  R75 *4.02K/F_4	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	(6) MCH_CFG_19  R72 *4.02K/F_4 +3V	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	(6) MCH_CFG_20  R73 *4.02K/F_4 +3V	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	(6,20) SDVO_CTRLDATA  R146 *2.2K/F_4 +3V	
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	(6,18) INT_LVDS_EDIDDATA  R166 *2.2K/F_4 +3V	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	(6) DDPC_CTRLDATA  R71 *2.2K/F_4 +3V	

Enable iTPM Table

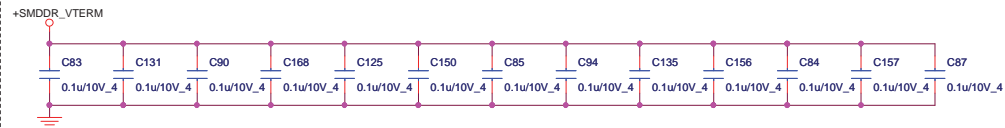
PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin


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Size	Document Number	Rev
	CLK. GEN./ CK505	1A
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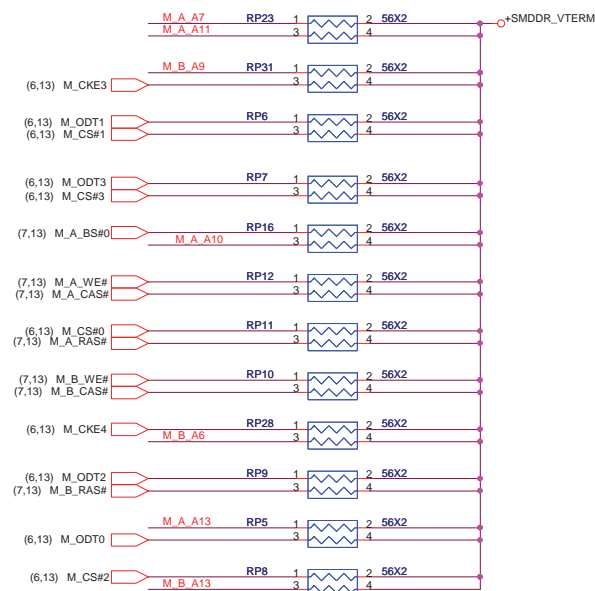
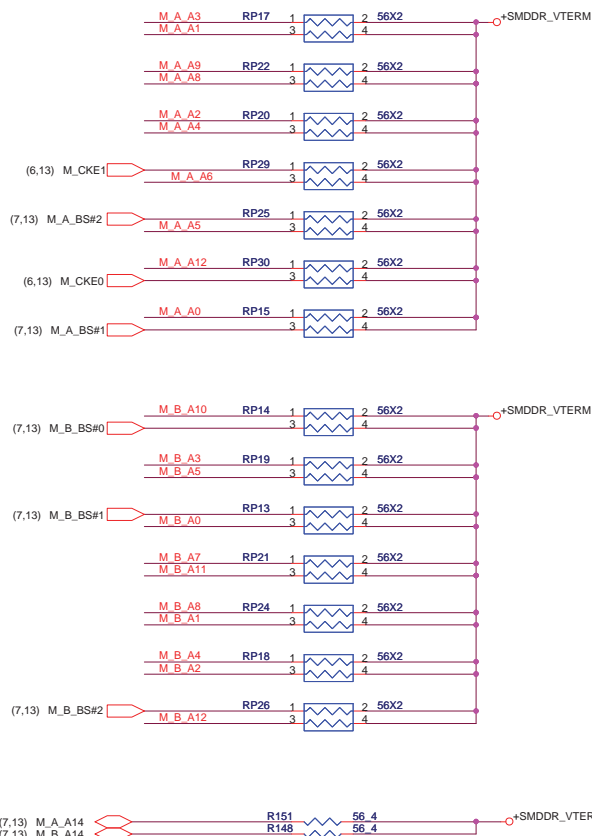
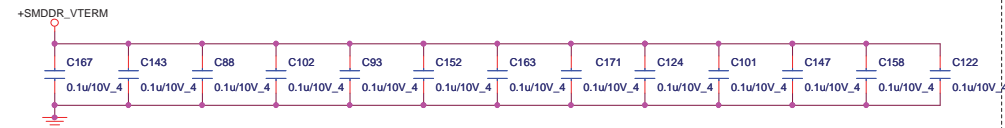
DDR2 Dual channel A/B PU


DDRII A CHANNEL



M_A_A[13..0] M_A_A[13..0] (7,13)
M_B_A[13..0] M_B_A[13..0] (7,13)

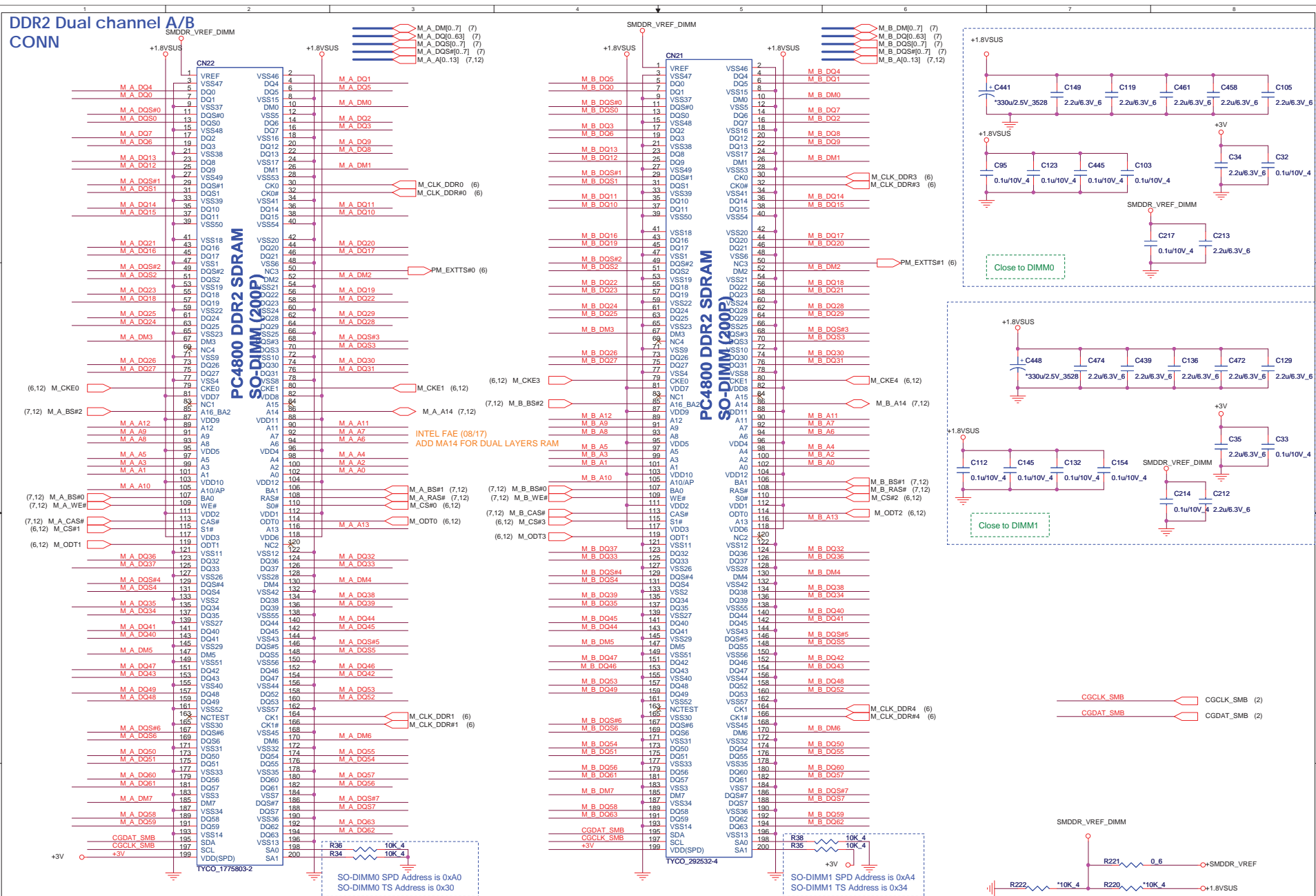
DDRII B CHANNEL




Quanta Computer Inc.
PROJECT : BL5M Montevina

Size	Document Number	Rev
	DDR RES. ARRAY	1A
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DDR2 Dual channel A/B CONN



Standard Type H: 6.5mm

CLOCK 0,1
CKE 0,1

Standard Type H: 11mm

CLOCK 3,4
CKE 2,3

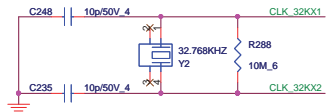
<http://hobi-elektronika.net>

Quanta Computer Inc.
PROJECT : BL5M Montevina

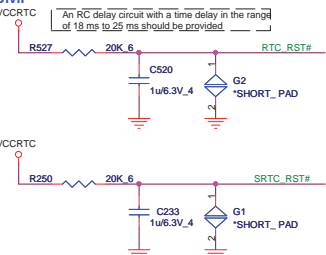
Size: Document Number: Rev: 1A
DDR SO-DIMM(200P)

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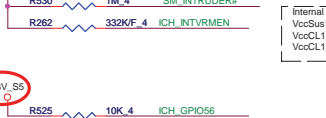
RTC CRYSTAL



RESET JUMP



VCCRRTC

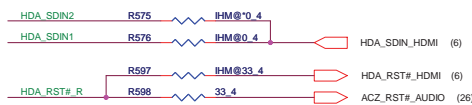


(DG 1.0 Table-292)







Internal VREF enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05.

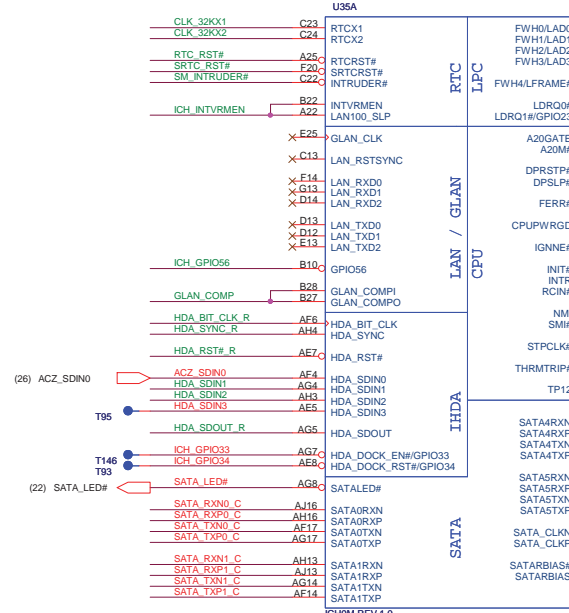
24.9 Ohm pull up to 1.5V for GLAN_COMP10 is required, no matter intel LAN is used or not.

HD Audio I/F(CODEC & iHDMI)

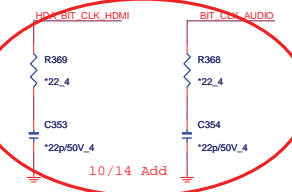


South Bridge Strap Pin (1/3)

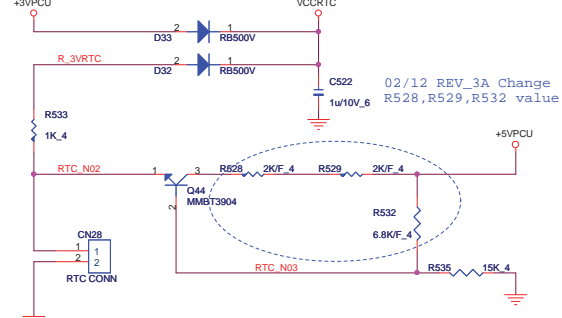
Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect			This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU			
TP3	XOR Chain Entrance	PWROK	ICH_TP3	HDA_SDOUT	Description	(16) ICH_TP3  ICH_TP3 R264  *1K_4 
			0	0	RSVD	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	0	1	Enter XOR Chain	 HDA_SDOUT_R R582  *1K_4  +3V_HDA_IO_ICH PU +1.5V
			1	0	Normal operation(Default)	
			1	1	Set PCIe port config bit 1	



SATA_RBIA5_PN<0.5". Avoid routing next to clock/high speed signals



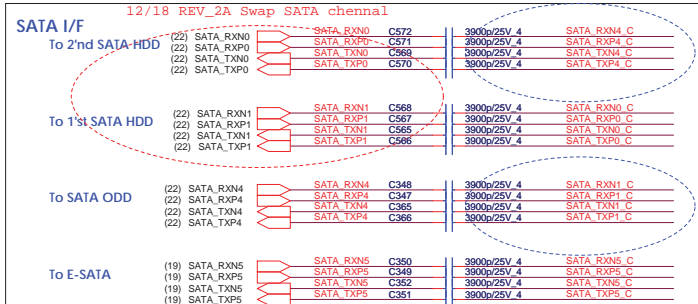
RTC BATTERY



BOM Option Table

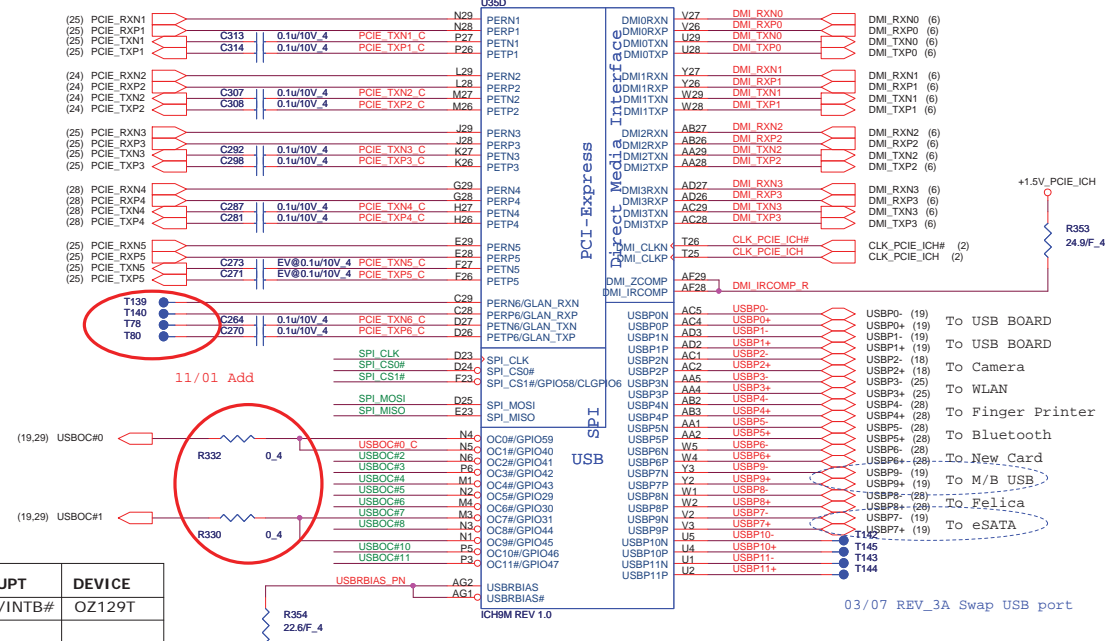
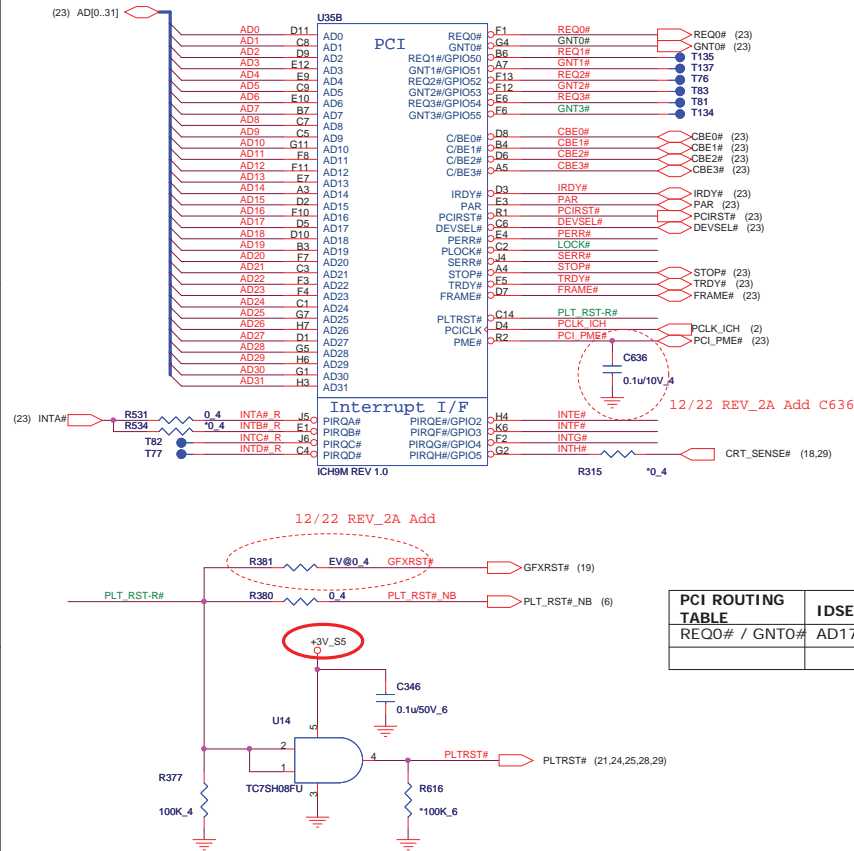
Reference	Description
IHM@	INT HDMI

02/14 REV_3A Swap SATA chennal



Quanta Computer Inc.
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Size: Document Number CLK_GEN/ CK505 Rev 1A
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PCI/PCI-E/USB/DMI/SPI

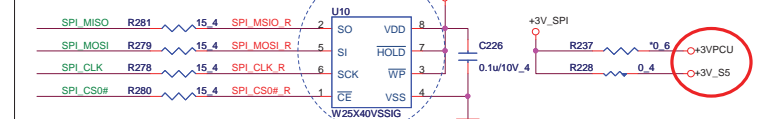


BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA# / INTB#	OZ129T

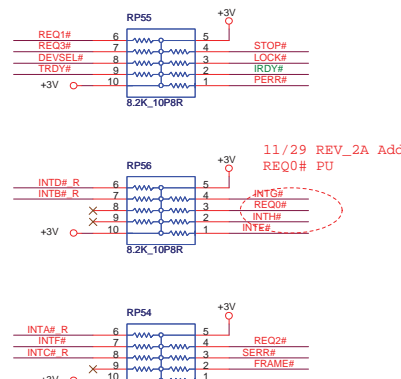
ITPM SERIAL EEPROM



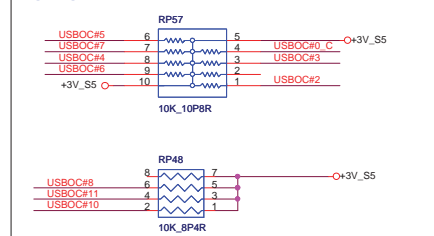
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD									
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0										
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default										
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default										
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	Enable iTPM 									
GNT0#	Boot BIOS Selection 0	PWROK	<table><tr><th>PCI_GNT#0</th><th>SPI_CS#1</th><th>Boot Location</th></tr><tr><td>0</td><td>1</td><td>SPI(Default)</td></tr></table>	PCI_GNT#0	SPI_CS#1	Boot Location	0	1	SPI(Default)				
PCI_GNT#0	SPI_CS#1	Boot Location											
0	1	SPI(Default)											
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	<table><tr><th>PCI_GNT#0</th><th>SPI_CS#1</th><th>Boot Location</th></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>1</td><td>1</td><td>LPC</td></tr></table>	PCI_GNT#0	SPI_CS#1	Boot Location	1	0	PCI	1	1	LPC	
PCI_GNT#0	SPI_CS#1	Boot Location											
1	0	PCI											
1	1	LPC											

PCI PULL-UP

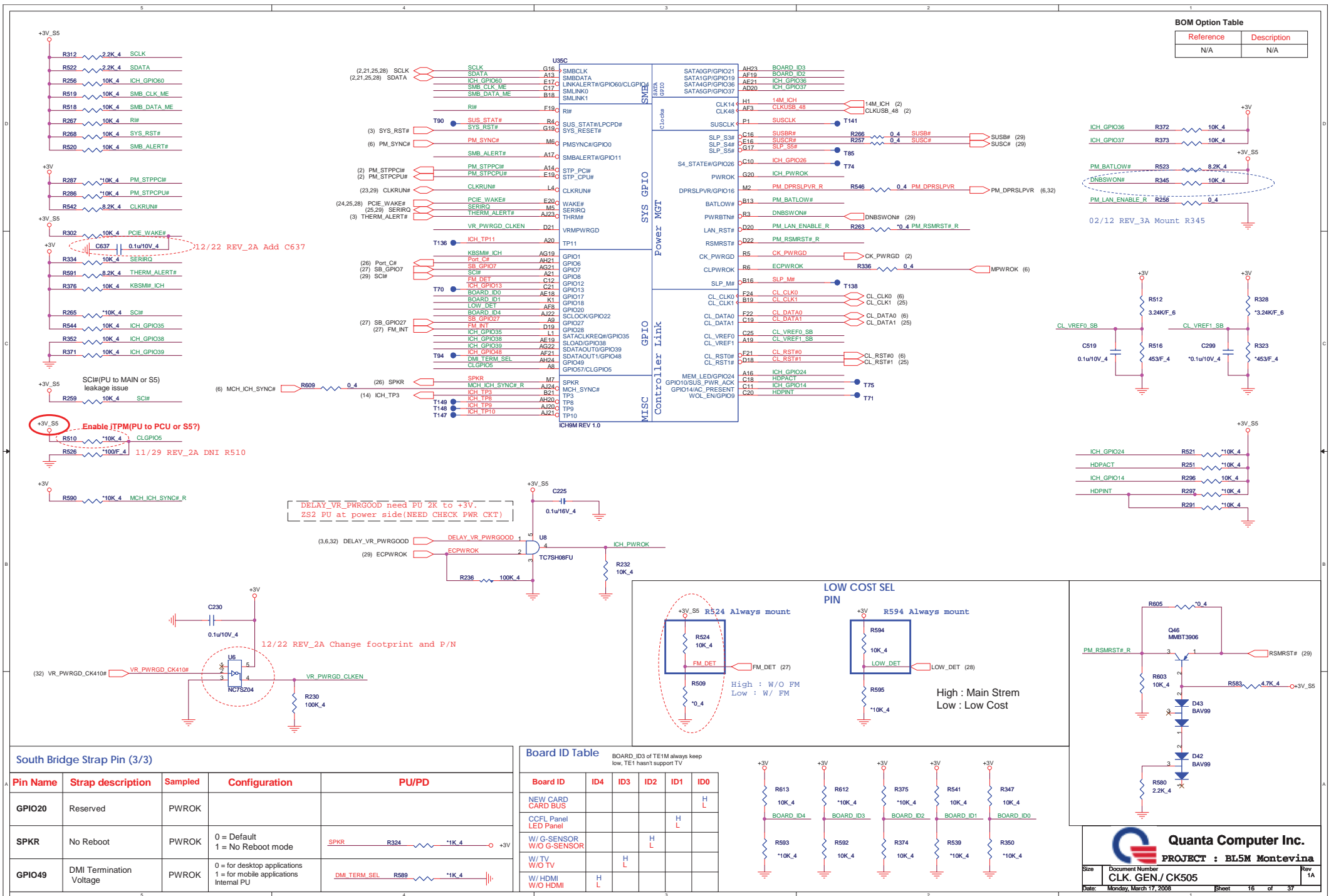


USB0# PULL-UP



Quanta Computer Inc.
PROJECT : BL5M Montevina

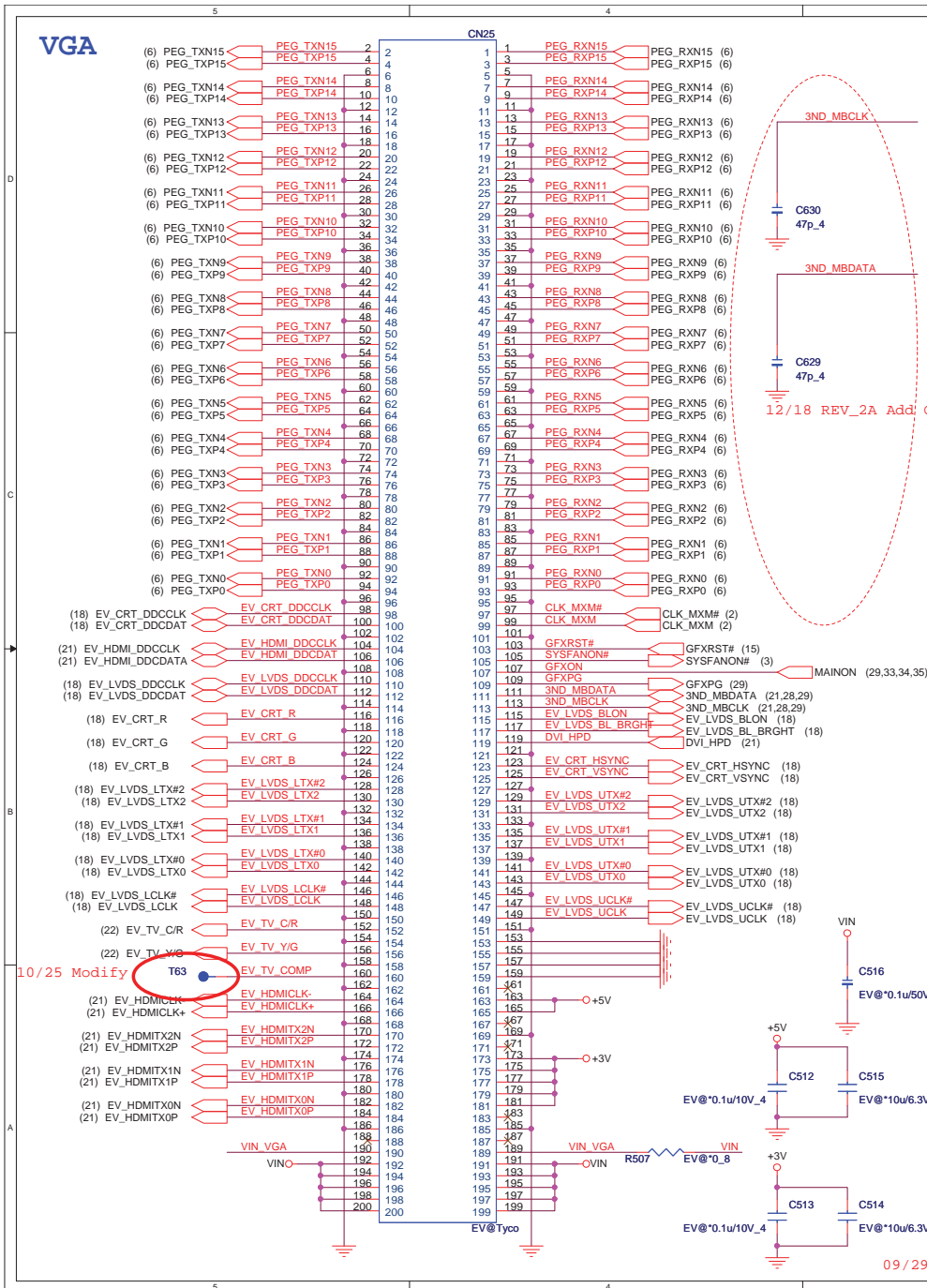
Size: Document Number: 1A
Date: Monday, March 10, 2008 Sheet 15 of 37



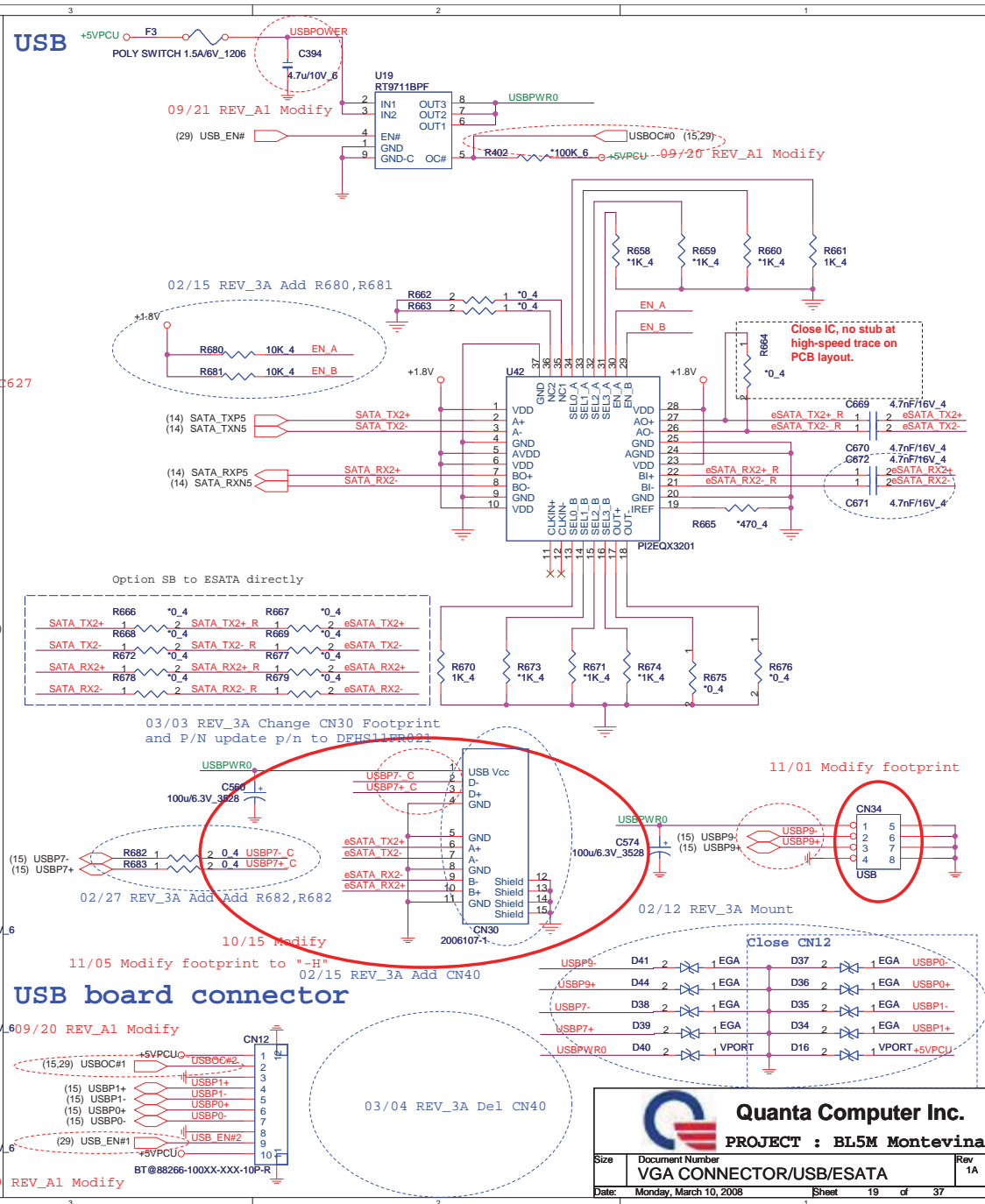
CRT PORT

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV&IV diff. value

VGA



USB



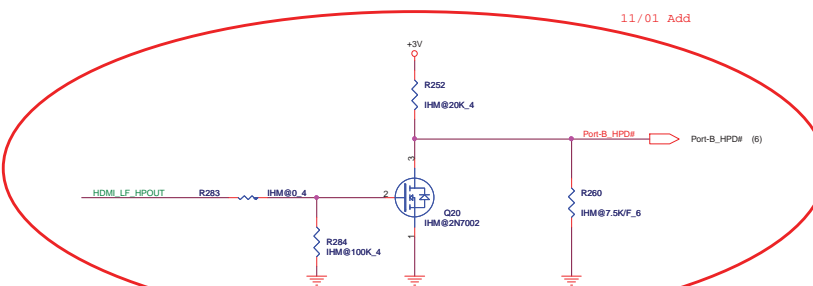
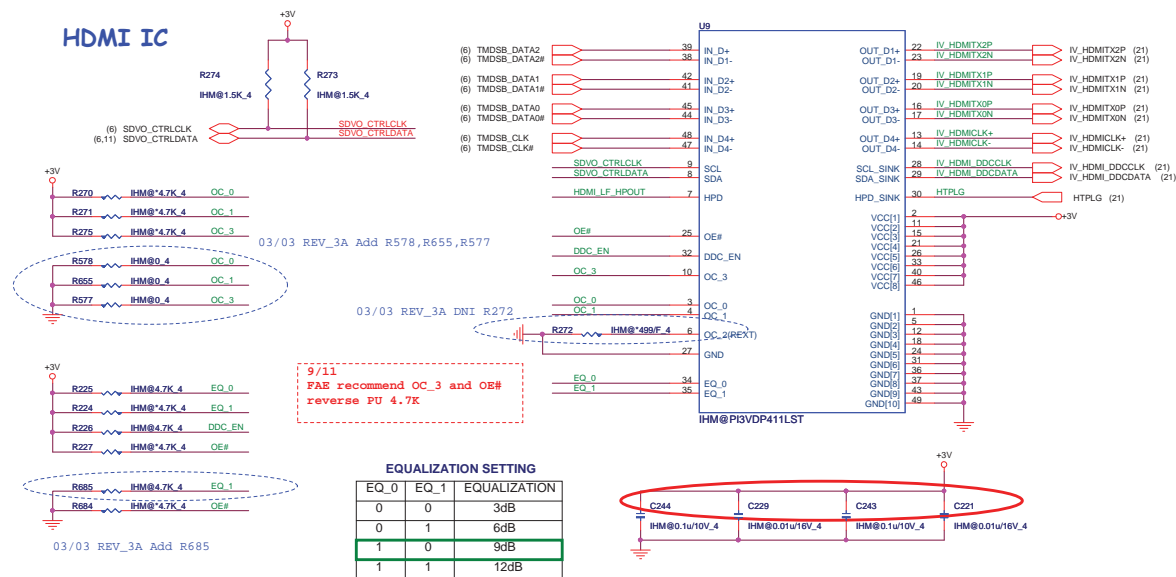
Quanta Computer Inc.

PROJECT : BL5M Montevina

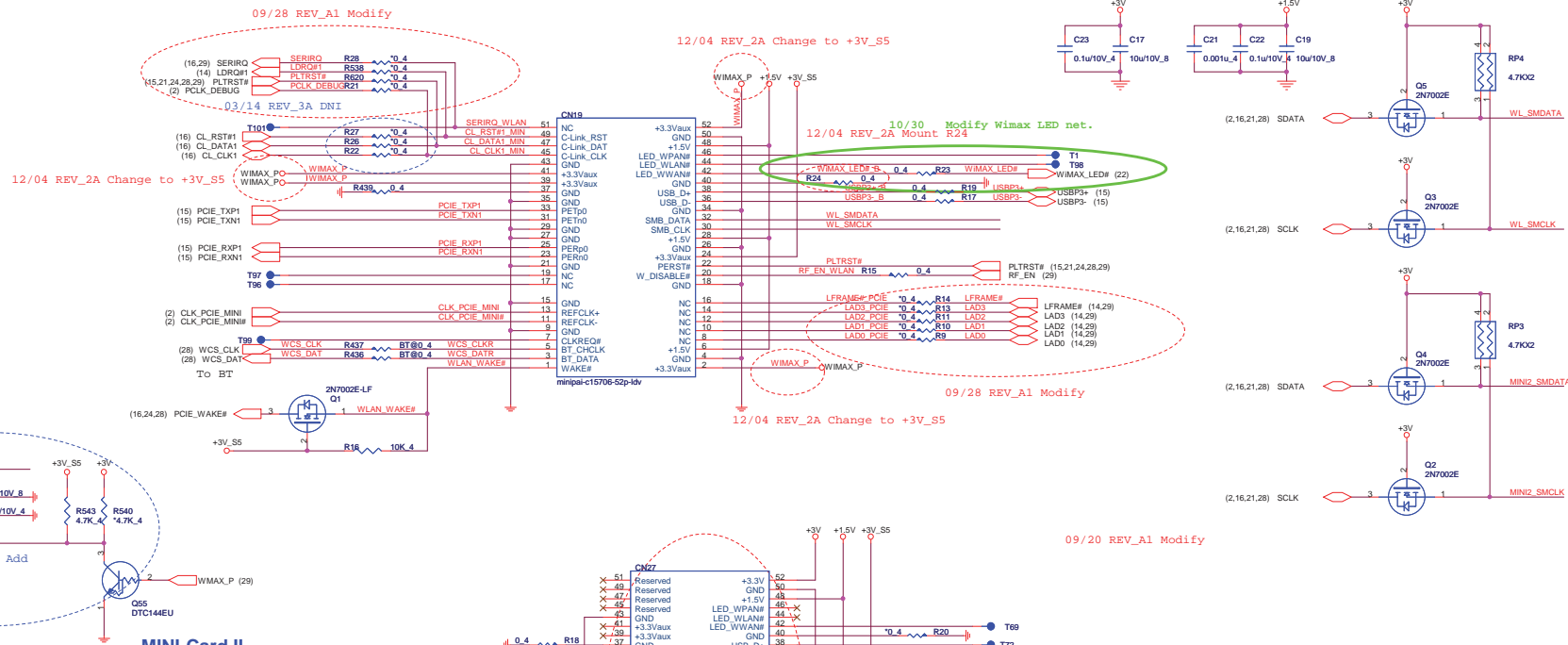
Size: Document Number
VGA CONNECTOR/USB/ESATA

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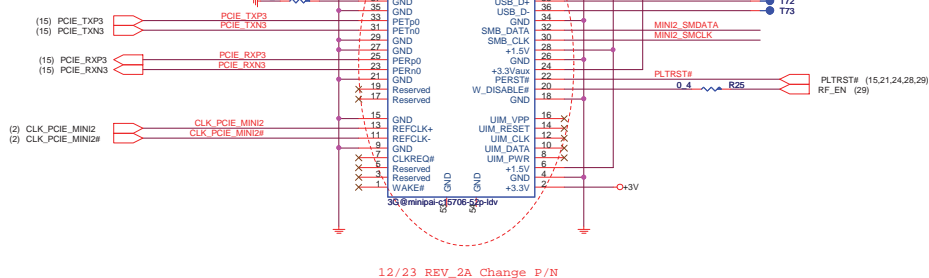
HDMI IC


<http://hobi-elektronika.net>

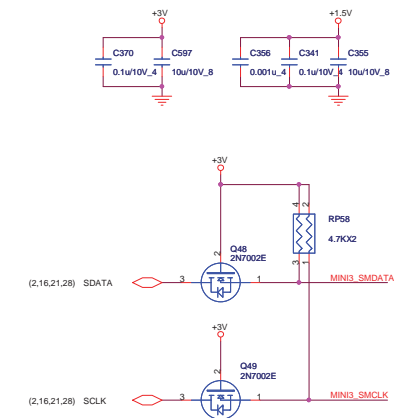
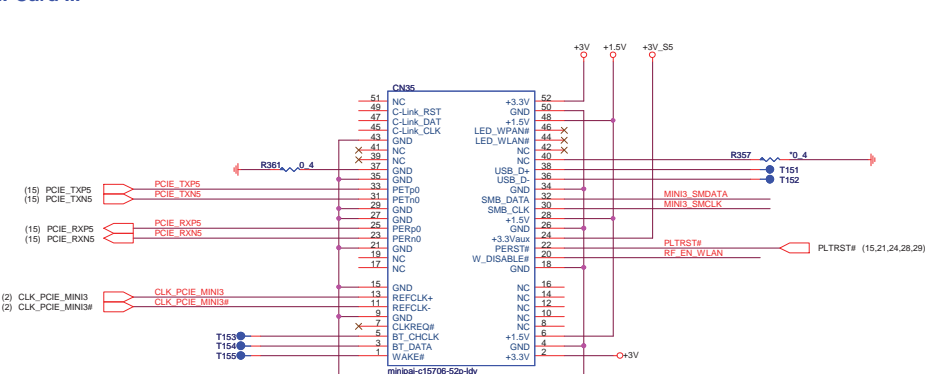
MINI-Card I

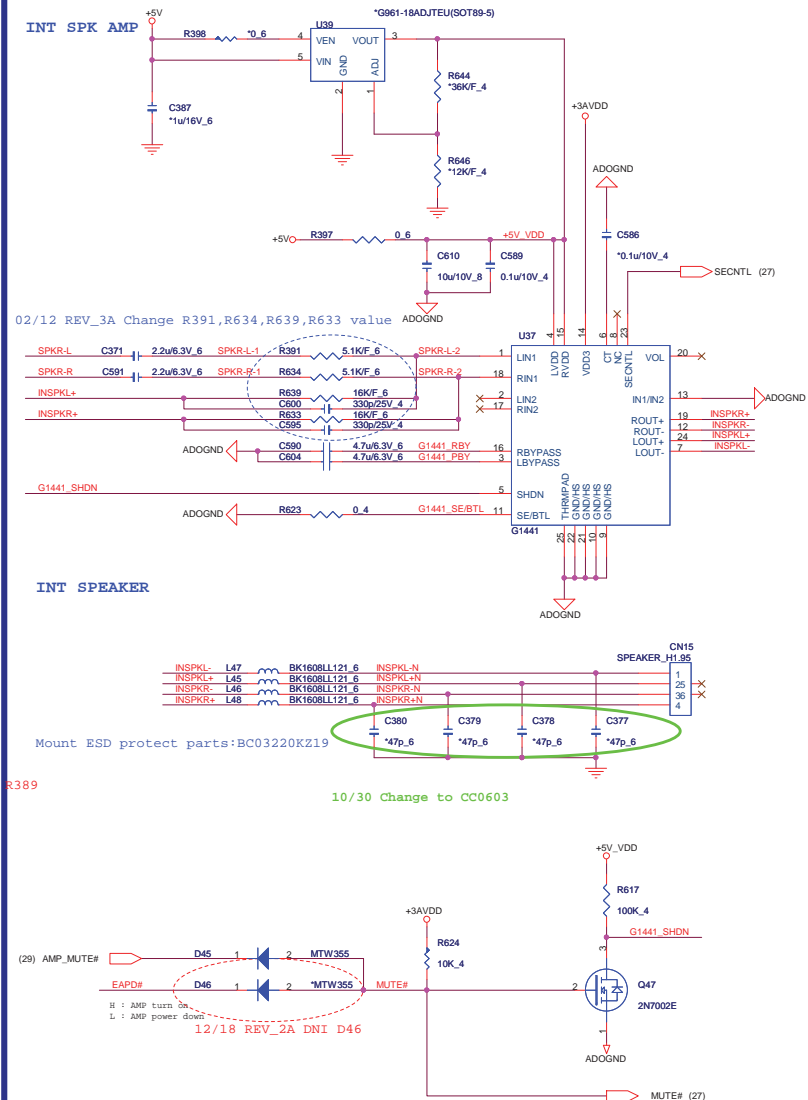
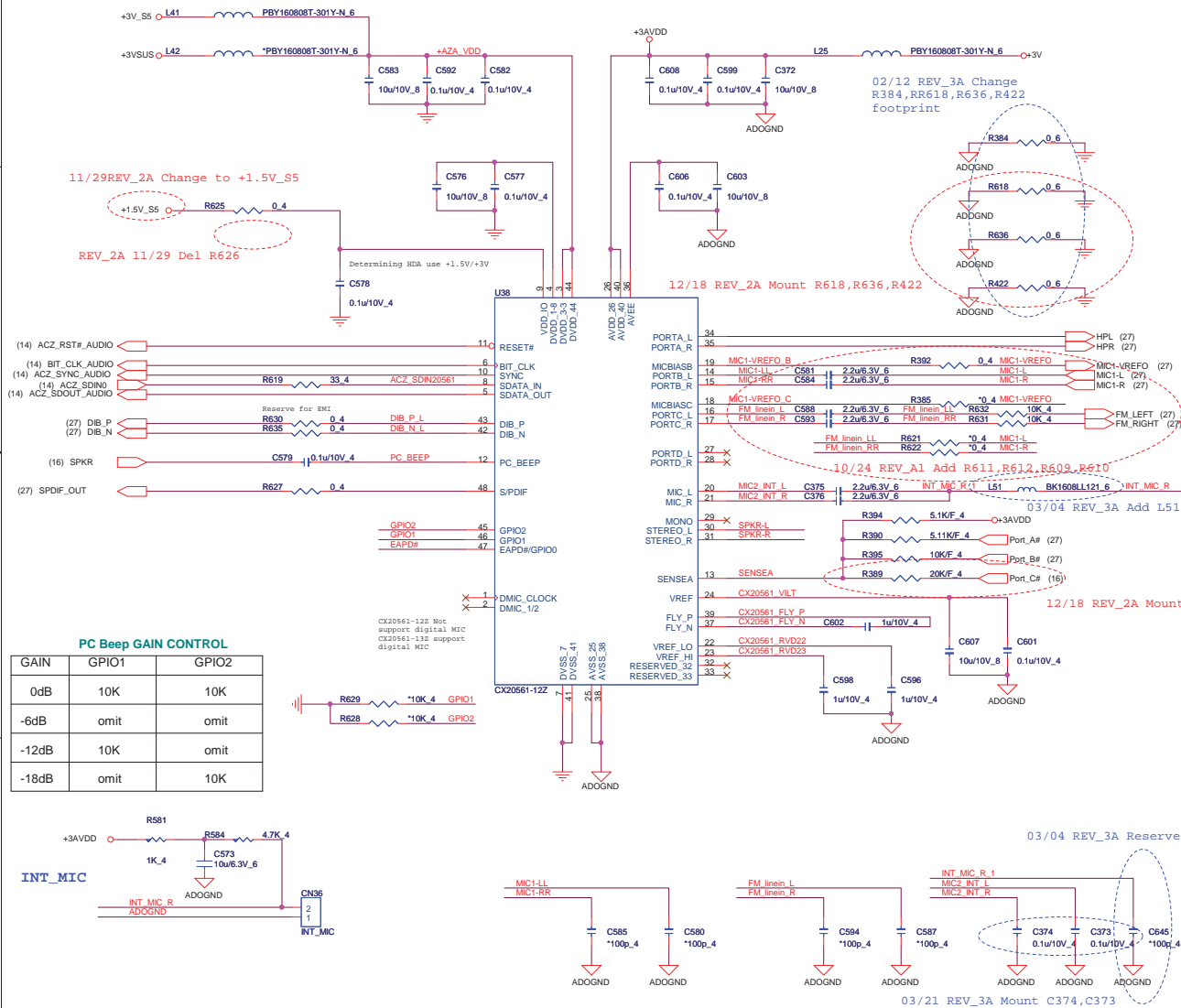


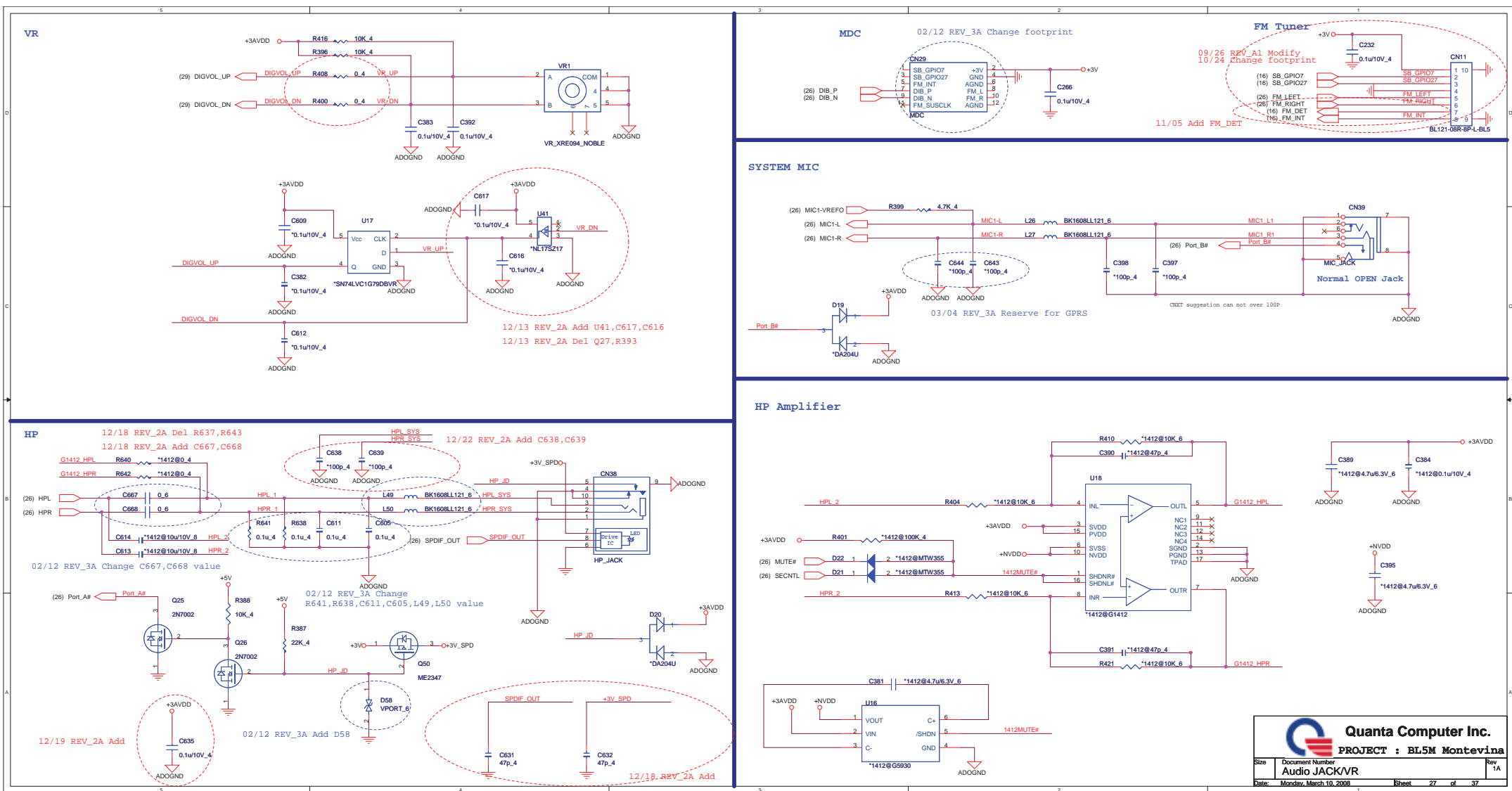
MINI-Card II

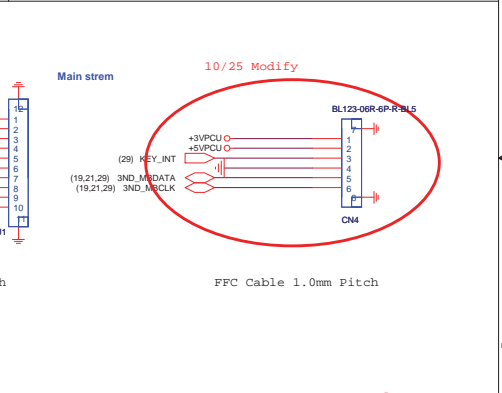
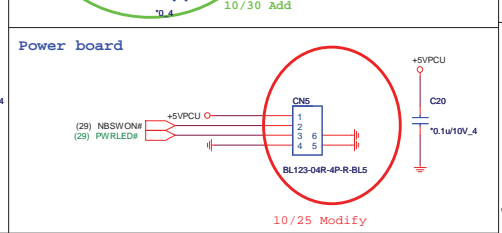
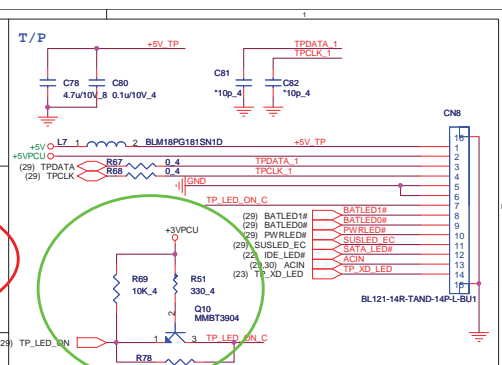


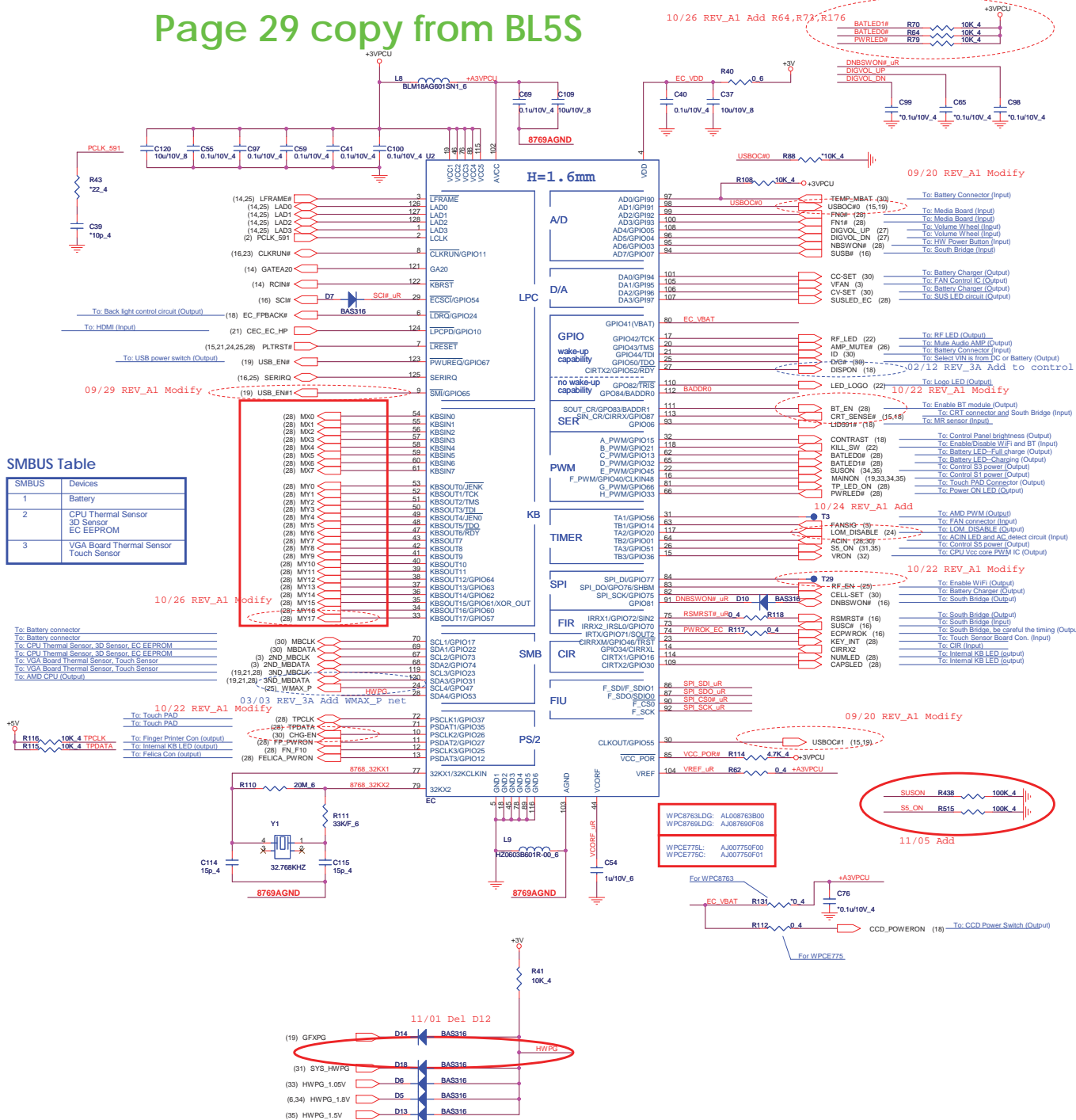
MINI-Card III



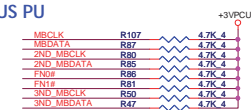








SM BUS PU



I/O Base Address

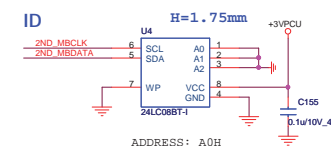
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MOD	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

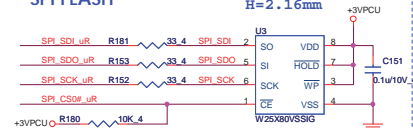


12/18 REV_2A R54 DNI,R5

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

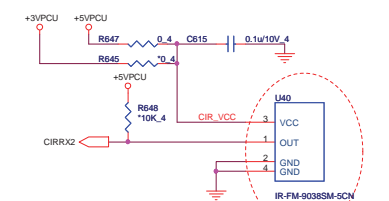


SPI FLASH

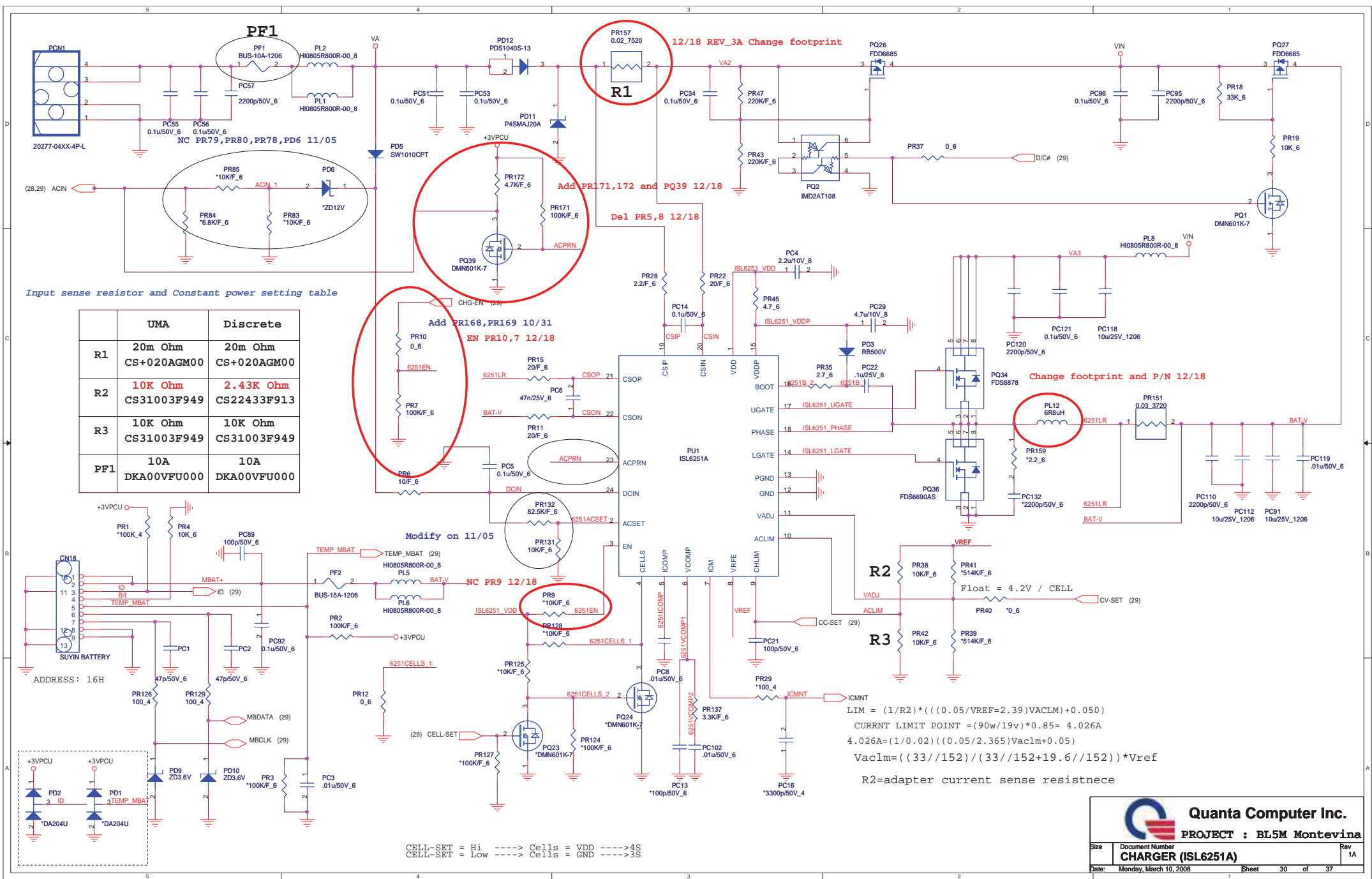


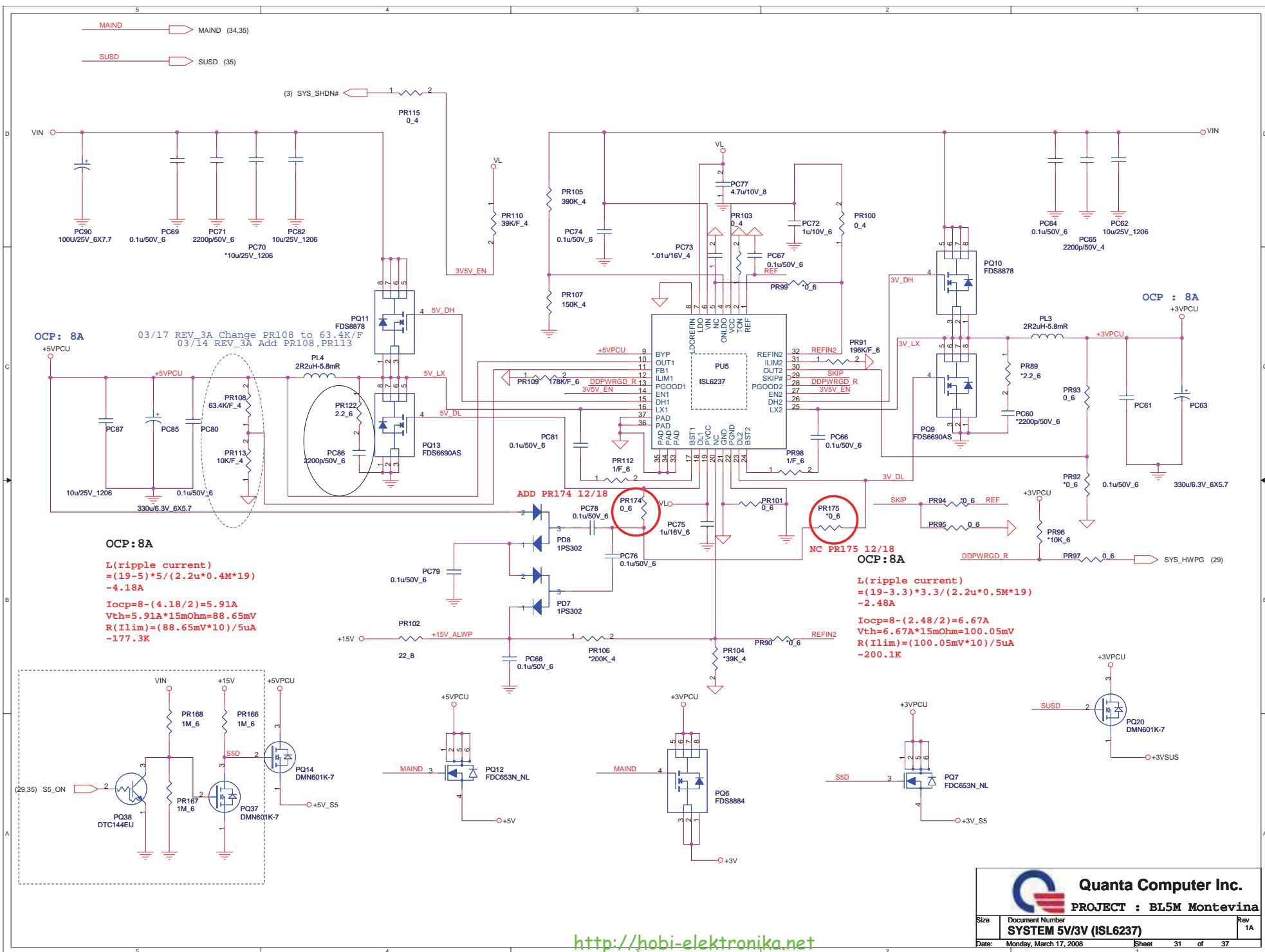
INTERNAL KEYBOARD STRIP SET

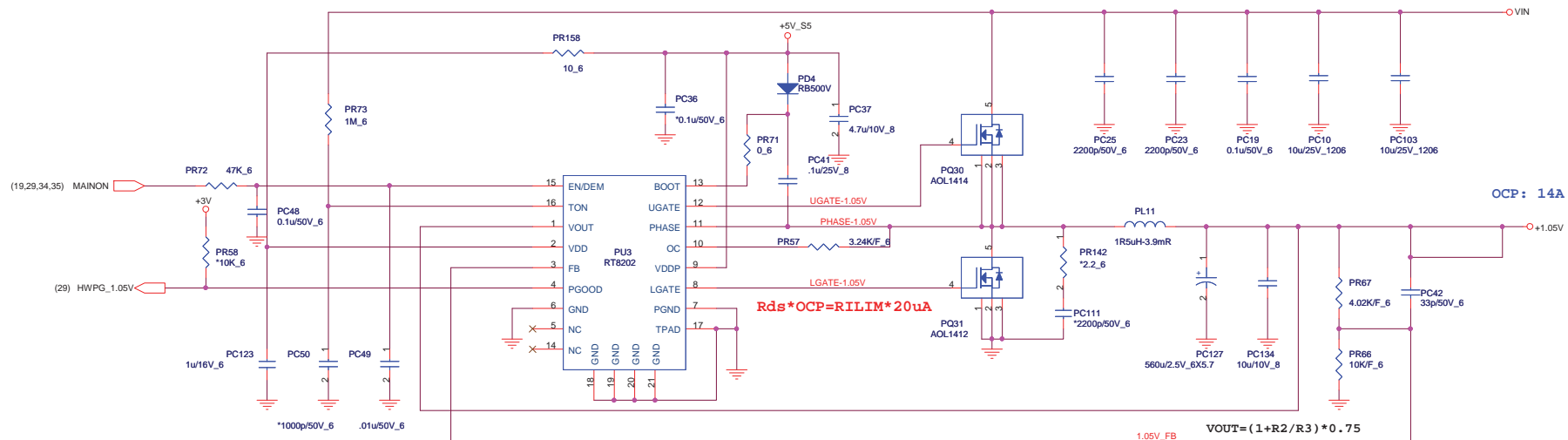
CIR (Copy from PB2A)
Only for 8769/775C

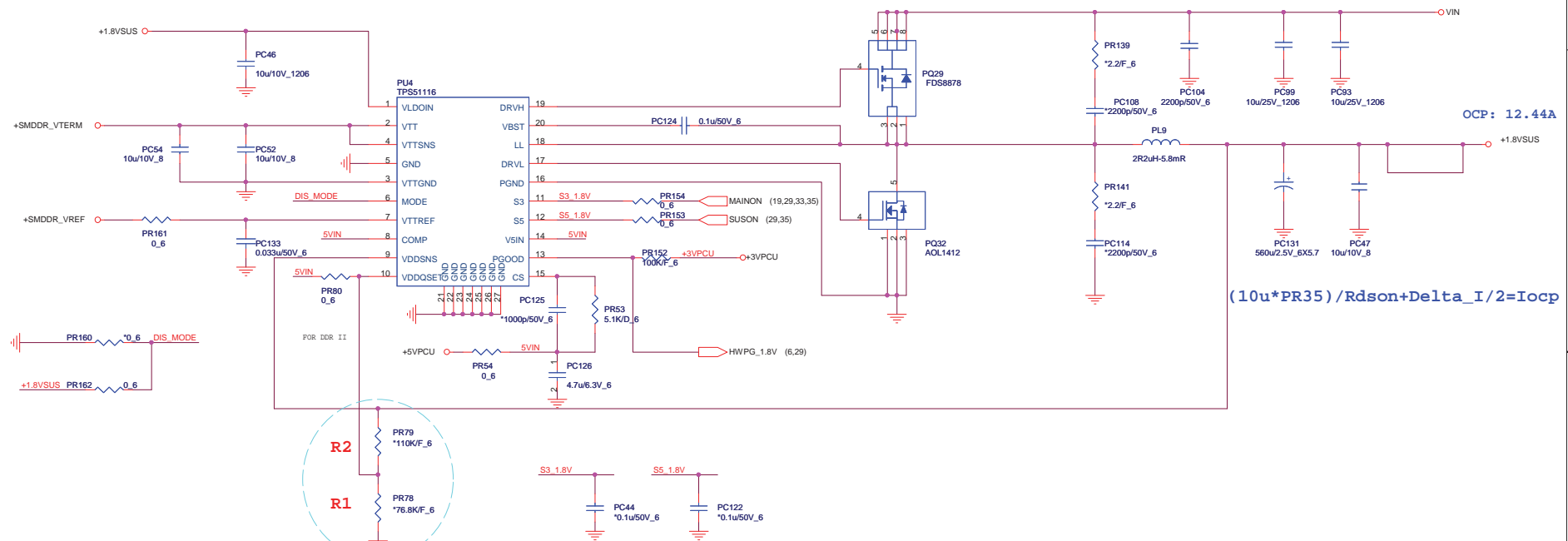


10/19 REV_A1 Change footprint
10/21 REV_A1 Change pin define



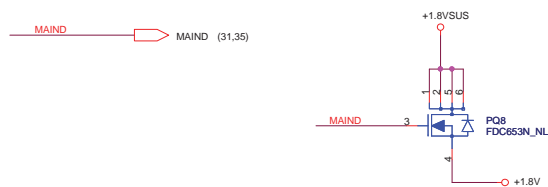


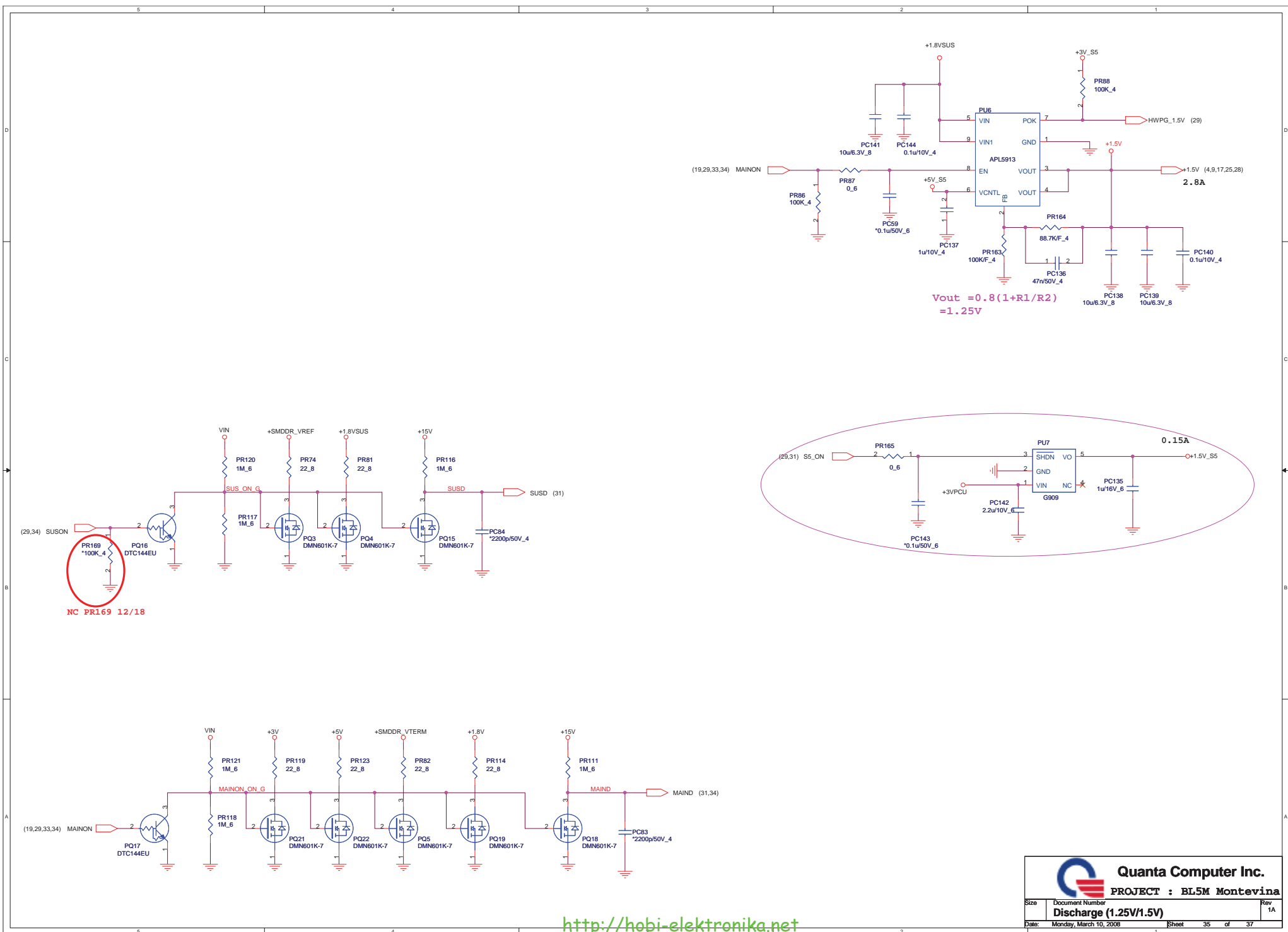




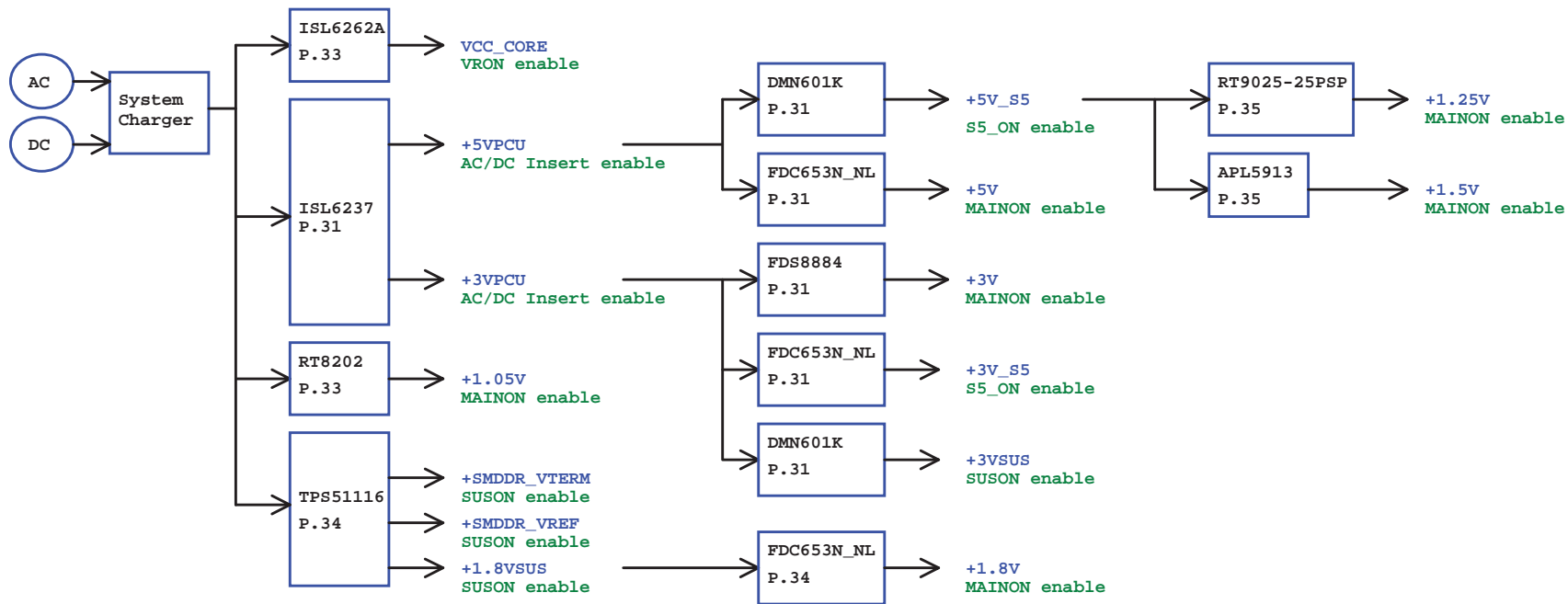
$$R1 = (100 \cdot V_{out} - R2) K$$

if tune Vout PR38 un-mount, PR156 PR165 mount





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Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T), Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M